ONS00470
10/773,853

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Grivna, Gordon M.
Serial No.:	10/773,853
Filing Date:	February 9, 2004
Group Art Unit:	2826
Examiner:	Fetsum Abraham
Title:	**SEMICONDUCTOR DEVICE HAVING REDUCED CAPACITANCE TO SUBSTRATE AND METHOD**

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13 pages

APPEAL BRIEF

I. REAL PARTY OF INTEREST

The real party of interest in this appeal is Semiconductor Components Industries, LLC (SCI), doing business as ON Semiconductor.

II. RELATED APPEALS AND INTERFERENCES

Applicants are not aware of any related appeals or interferences to this application.

III. STATUS OF THE CLAIMS

Claims 1-20 are in the proceeding. Claims 10-20 are the claims on appeal. A copy of the claims on appeal is provided in Section VIII., Claims Appendix.

Claims 1-9 are canceled.
Claims 10-20 are rejected.

IV. STATUS OF THE AMENDMENTS

An amendment was filed on September 22, 2004 and entered into the record. A second amendment was filed on November 8, 2004 and entered into the record. A Response to the Final Rejection was filed on May 4, 2005 but was not entered into the record. An Amendment on Appeal canceling claims 1-9 is filed concurrently with this Appeal Brief as allowed pursuant to 37 CFR § 41.33 (b).

V. SUMMARY OF CLAIMED SUBJECT MATTER

Claim 10 calls for a process for forming an integrated circuit device (33), as described on page 4, line 19 through page 5, line 12, and as shown in FIG. 1, including the step of forming a tub region (10) within a semiconductor layer (30), wherein tub region (10) includes a matrix of shapes (13) comprising offset rows (121 and 122). Claim 10 further calls for forming a dielectric region (15) within the matrix of shapes (13). As

described on page 3, lines 31-34, the matrix of shapes (13) are formed in offset rows (121 and 122) to minimize the void or air gap formation and high stresses during a thermal oxidation or dielectric growth which forms dielectric region (15).

Claim 12 calls for the process of claim 10 wherein the step of forming the dielectric region (115) includes oxidizing the matrix of shapes (13). This process is described in detail in applicant's specification on page 7, lines 22-26, with reference to FIG. 7.

Claim 13 calls for the process of claim 12 wherein the step of oxidizing forms a nearly continuous silicon oxide tub (10). This process is described in detail in applicant's specification on page 7, lines 26-34, with reference to FIG. 7.

Claim 18 calls for a semiconductor device (33), as described on page 4, line 19 through page 5, line 12, and as shown in FIG. 1, comprising a region of semiconductor material (30), a dielectric tub (10) formed in the region of semiconductor material (), wherein the dielectric tub (10) includes a matrix of passivated shapes (13), and wherein adjacent rows (121 and 122) of passivated shapes (13) are offset. As described on page 3, lines 31-34, the matrix of shapes (13) are formed in offset rows (121 and 122) to minimize the void or air gap formation and high stresses during a thermal oxidation or dielectric growth which forms dielectric region (15).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Rejection of claims 10 and 12-16 under 35 U.S.C. §103 as being unpatentable over Wieczorek et al., USP 6,821,840, (hereinafter "Wieczorek").

B. Rejection of claims 10-20 under 35 U.S.C. §103 as being unpatentable over Burns et al., USP 6,034,389, (hereinafter "Burns")

VII. ARGUMENT

A. Arguments for allowability of Claims 10 and 12-16 over Wieczorek.

1. Arguments for allowability of Claims 10 and 14-16.

Applicants respectfully submit that Wieczorek fails to make claim 10 obvious for the following reasons.

Claim 10 calls for, a process for forming an integrated circuit device including forming a tub region within a semiconductor layer, wherein tub region includes a matrix of shapes comprising offset rows. The method further calls for forming a dielectric region within the matrix of shapes. Applicant's FIGs. 1 or 2 illustrates the matrix of shapes (such as pillars, protrusions, or posts) comprising offset rows, clearly showing that shapes 13 are offset from each other in adjacent rows (in other words, when looking at applicant's structure from the top, the center of the shapes in the second row are not formed in a straight line from the center of the shapes in the first row). By providing the adjacent rows of shapes offset from each other, void or air gap formation and high stresses are minimized (see applicant's specification on p. 3, l. 31-34), which improve reliability and device performance. As stated in applicant's specification on p. 4, l. 7-9, voids or air gaps have been shown to cause significant problems in prior art structures.

Applicant respectfully submits that Wieczorek fails to make claim 10 obvious because Wieczorek does not show nor suggest a method of forming an isolation region including forming a tub region including a matrix of shapes comprising offset rows.

Specifically, Wieczorek is completely silent as to how structures 120 (or 220) are positioned. Wieczorek does not disclose that his structures be formed as a matrix of shapes formed in offset rows from each other. The reference also does not provide any motivation or suggestion to form the regions 120 (or 220) in a matrix of offset rows. For at least these reasons, applicant respectfully submits that claim 10 is allowable over Wieczorek.

Claims 14-16 depend from claim 10 and are believed allowable for at least the same reasons as claim 10.

2. Arguments for allowability of Claim 12.

Claim 12 calls for the step of forming the dielectric region (within the matrix of shapes) to include oxidizing the matrix of shapes. The Examiner states that Wieczorek shows isolation regions 102 or 202 are oxidized shapes making a matrix and the step of oxidizing them forms a continuous oxide layer of isolation trenches vertically. However, Wieczorek is not believed to teach oxidizing the shapes 120 or 220 to form isolation regions 102 or 202. In col. 2, lines 23-27, Wieczorek states only that sophisticated photolithography and etch techniques are used for defining the isolation structures 102. Wieczorek does not provide any motivation or suggestion to oxidize the shapes 120 or 220, and in fact, doing so would likely alter the device characteristics of Wieczorek's device and may render it unworkable. Therefore, claim 12 is not believed to be obvious over Wieczorek.

3. Arguments for allowability of Claim 13.

Claim 13 calls for the step of oxidizing of claim 12 to form a nearly continuous silicon oxide tub. The Examiner states that Wieczorek shows isolation regions 102 or 202 are oxidized shapes making a matrix and the step of oxidizing them forms a continuous

oxide layer of isolation trenches vertically. Applicants have shown that the isolation regions of Wieczorek are not formed by oxidation, as argued above with respect to claim 12. In addition, Wieczorek does not show a nearly continuous silicon oxide tub as called for in claim 13. The semiconductor region (shape) 120 is always a significant portion of the tub in all of Wieczorek's embodiments. Wieczorek does not provide any motivation or suggestion to use the method claimed by applicant. Therefore, claim 13 is believed to be allowable.

B. Arguments for allowability of claims 10-20 over Burns.

1. Arguments for allowability of claims 10, 11, and 14-17.

Claim 10 calls for, a process for forming an integrated circuit device including forming a tub region within a semiconductor layer, wherein tub region includes a matrix of shapes comprising offset rows. As described above, Applicant's FIG. 1 or 2 illustrates this feature, clearly showing that shapes 13 are offset from each other in adjacent rows. By providing the adjacent rows of shapes offset from each other, void or air gap formation and high stresses are minimized, which improve reliability and device performance.

Applicant respectfully submits that Burns fails to make claim 10 obvious because Burns does not show nor suggest a method of forming a matrix of shapes comprising offset rows. The shapes or pillars of Burns are not offset from each other in each adjacent rows (see any perspective figure, including, at least, FIGs. 1, 2, 4, 36, 40, and 44). The Examiner refers to FIG. 41, however, FIG. 41 is not in perspective view. Burns indicates that FIGs. 36-44 (see col. 7, line 44) illustrate an embodiment of his invention. FIGs. 36, 40, and 44 (and thus FIG. 41) all show shapes which are not formed in offset rows. Burns clearly

teaches away from applicant's invention and thus cannot support a basis for an obviousness rejection. In addition, Burns does not provide any suggestion or motivation to alter the formation of his shapes so that they are formed offset from each other, as applicant's claim. For at least these reasons, applicant respectfully submits that claim 10 is allowable over Burns.

Claims 11 and 14-17 depend from claim 10 and are believed allowable for at least the same reasons as claim 10.

2. Arguments for allowability of Claim 12.

Claim 12 calls for the step of forming the dielectric region (within the matrix of shapes) to include oxidizing the matrix of shapes. The Examiner states that dielectric regions 270 in Burns are oxides and are vertically continuous. However, Burns is not believed to teach oxidizing to form the dielectric regions 270. In col. 13, line 65 through col. 14, line 7, Burns states that "the second dielectric layer is a deposited silicon dioxide, referred to as a control or gate oxide 270. (emphasis added)" In addition, Burns does not provide any motivation or suggestion to oxidize the shapes 120 or 220. Therefore, claim 12 is not believed to be obvious over Burns.

3. Arguments for allowability of Claim 13.

Claim 13 calls for the step of oxidizing of claim 12 to form a nearly continuous silicon oxide tub. The Examiner states that dielectric regions 270 in Burns are oxides and are vertically continuous. Applicants have shown that the dielectric layers 270 of Burns are not formed by oxidation, as argued above with respect to claim 12. In addition, Burns does not show a nearly continuous silicon oxide tub as called for in claim 13. The pillars 230 are always a significant portion of the tub in all of Burns's embodiments. Furthermore, Burns does not provide any

motivation or suggestion to use the method claimed by applicant. Therefore, claim 13 is believed to be allowable.

4. Arguments for allowability of claims 18-20.

Claim 18 calls for a semiconductor device including a region of semiconductor material. A dielectric tub is formed in the region of semiconductor material, wherein the dielectric tub includes a matrix of passivated shapes, and wherein adjacent rows of passivated shapes are offset.

Applicant respectfully submits that Burns fails to make claim 18 obvious because Burns does not show nor suggest a device having a dielectric tub which includes a matrix of passivated shapes, and wherein adjacent rows of passivated shapes are offset. The shapes or pillars of Burns are not offset from each other in each adjacent row (see any perspective figure, including, at least, FIGs. 1, 2, 4, 36, 40, and 44). Burns clearly teaches away from applicant's invention and thus cannot support a basis for an obviousness rejection. Burns does not provide any suggestion or motivation to alter the formation of his shapes so that they are formed offset from each other, as applicant's claim. For at least these reasons, applicant respectfully submits that claim 18 is allowable over Burns.

Claims 19-20 depend from claim 18 and are believed allowable for at least the same reasons as claim 18.

In view of the above, it is believed that the claims are allowable, and the Board of Appeals and Interferences is respectfully requested to reverse the Examiner.

Respectfully submitted,
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VIII. CLAIMS APPENDIX

1. (canceled): A method for forming an isolation region comprising the steps of:

providing a region of semiconductor material;

forming a tub in the region of semiconductor material, wherein the tub includes a plurality of shapes; and

exposing the plurality of shapes to an ambient that includes a chemical species that reacts with the plurality shapes to form the isolation region, and wherein the plurality of shapes form part of the isolation region.

2. (canceled): The method of claim 1 wherein the step of exposing includes thermally oxidizing the plurality of shapes to form a silicon oxide isolation region.

3. (canceled): The method of claim 1 wherein the step of forming the tub includes forming the tub having a boundary around the plurality of shapes, wherein the boundary includes a recessed portion.

4. (canceled): The method of claim 1 wherein the step of exposing includes consuming substantially all of the plurality of shapes.

5. (canceled): The method of claim 1 further comprising the step of forming a passive device over the isolation region.

6. (canceled): The method of claim 1 wherein the step of forming the tub includes etching exposed portions of the region of semiconductor material, and wherein the plurality of shapes comprise unexposed portions of the region of semiconductor material.

7. (canceled): The method of claim 6 wherein the step of etching includes etching to a depth from about 6 microns to about 10 microns.

8. (canceled): The method of claim 1, wherein the step of forming the tub includes forming a tub having a matrix of free standing shapes, wherein adjacent rows of shapes are offset from each other.

9. (canceled): The method of claim 1 wherein the step of providing the region of semiconductor material includes providing a region comprising silicon.

10. (previously presented): A process for forming an integrated circuit device including the steps of:

forming a tub region within a semiconductor layer, wherein tub region includes a matrix of shapes comprising offset rows; and

forming a dielectric region within the matrix of shapes.

11. (previously presented): The process of claim 10 wherein the step of forming the tub region includes forming a tub region with a matrix of squares.

12. (original): The process of claim 10 wherein the step of forming the dielectric region includes oxidizing the matrix of shapes.

13. (original): The process of claim 12 wherein the step of oxidizing forms a nearly continuous silicon oxide tub.

14. (original): The process of claim 10 further comprising the step of forming a passive component over the dielectric region.

15. (original): The process of claim 10 further comprising the step of forming an isolation trench in the region of semiconductor material.

16. (original): The process of claim 10 further comprising the steps of:

forming a dielectric layer on sidewalls of the matrix of shapes; and

forming a polycrystalline semiconductor layer over the dielectric layer.

17. (previously presented): The process of claim 10 wherein the step of forming tub region includes forming tub region having a matrix of shapes wherein shapes in a first row have a first spacing, and wherein the shapes in the first row have a second spacing from shapes in a second row, and wherein the second spacing is less than the first spacing.

18. (previously presented): A semiconductor device comprising:

a region of semiconductor material; and

a dielectric tub formed in the region of semiconductor material, wherein the dielectric tub includes a matrix of passivated shapes, and wherein adjacent rows of passivated shapes are offset.

19. (original): The device of claim 18 wherein the dielectric tub comprises oxidized silicon shapes.

20. (original): The device of claim 18 wherein the dielectric tub includes a boundary having a recessed portion.

IX. EVIDENCE APPENDIX

No evidence has been submitted pursuant to § 1.130, 1.131, 1.132.

X. RELATED PROCEEDINGS APPENDIX

The appellant is not aware of any related proceedings.